The Teledyne e2v CIS124 LVSM sensor for large telescopes- design and prototype tests

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ABSTRACT

Teledyne e2v has designed and prototyped a large-format, high rate sensor with excellent read-noise and high quantum efficiency. The LVSM (or CIS124) sensor development has been funded by the European Southern Observatory for use on their Extremely Large Telescope.
The CMOS sensor is anticipated to be valuable for use on other large telescopes for adaptive optics and similar high-rate and low signal applications.
We describe the considerations that led to this CMOS sensor concept and then outline the specifications and design details of this back-illuminated, Peltier-cooled sensor. Key features include- 800x800 pixels, at least 700 frames/second, digital implementation, 9 or 10 bits, plus four analogue gains programmable by region, peak QE of 90% at 700 nm, less than 3 e- read-noise, programmable rolling shutter to allow S-H and pyramid WFS. The sealed package includes Peltier-cooling and mounting features for incorporation into a wavefront sensor camera.
We report on front-illuminated tests which validate electrically the design and includes electro-optical data.

Keywords: LVSM, CIS124, Wavefront sensing, High performance visible CMOS sensors, back side illuminated, Peltier-cooling package.

1. INTRODUCTION

This paper presents the Large Visible Adaptive optics Sensor Module (LVSM – CIS124), a high performance visible CMOS sensor that Teledyne e2v is developing for European Southern Observatory (ESO). The LVSM forms part of the LISA WFS camera designed by ESO to be used in multiple instruments and focal positions on the Extreme Large Telescope for different wavefront sensing (WFS) applications. In this case a large area CMOS sensor with large pixel pitch is required to operate at high frame rate with low noise specification and high quantum efficiency (QE). Table 1 below summarises the top level requirements for LVSM.

Table 1. Target specification for LVSM – CIS124.

Parameter	Specification
Array Format	800 x 800 pixels
Pixel Size	24 µm
Wavelength	460-950nm
Frame Rate	700 fps

Read out noise	< 3 e- rms
QE	> 80 %
Dark Current	< 0.5 e-/s/pixel at -5˚C
Storage Capacity	≥ 4000e-/pixel
Cosmetics	< 0.1%
Package format	Integral Peltier

This paper will start reviewing the different aspects of the die and package design. Then it will describe the key package assembly process and the equipment used for characterising the devices. We will conclude presenting the results obtained from the characterisation of the front face devices.

2. DIE DESIGN OVERVIEW

The LVSM has an image area of 800 x 800 pixels with additional 2 x 8 rows and 2 x 20 columns of dark reference pixels. A light shield is used on top of the back surface to cover the dark pixels and periphery and the sensor is back illuminated for high QE and good intra-pixel uniformity. Four high precision (<2 μm) alignment marks are placed on the silicon at each corner of the pixel array to assist in alignment of lenslet arrays to be mounted external to the package by ESO.

Figure 1 shows the floorplan and the parallel architecture with rows scanned in opposite directions, from the middle out, which makes it suitable for Shack-Hartmann WFS. Alternatively, the bottom half can also be scanned in the same direction as the top which is compatible with Pyramid WFS.

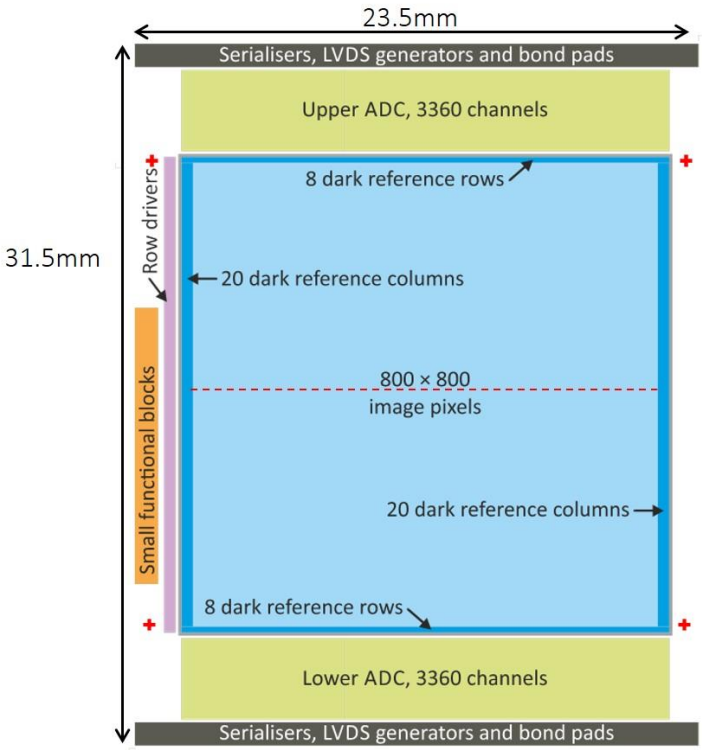

Figure 1. LVSM – CIS124 Floorplan

The CMOS sensor has on-chip ADC giving digital outputs in Low-Voltage Differential Signaling (LVDS); twenty LVDS output ports for the image and four for the reference pixel columns. By using the large pixel pitch, 24 μm, four ADCs can be placed side by side per pixel pitch. This allows a single row of ADCs per side (top and bottom) of the pixel array, minimising the risk of cross-talk inherent to approaches where multi-rows of ADC are used. The ADC resolution defined by 9 or 10 bits plus programmable analogue gain (×1, ×2, ×4 and ×8) and Correlated Double Sampling (CDS).

The CIS124 uses a 4T pixel type allowing rolling shutter operation mode for lowest noise. Figure 2 shows the readout path based on a column parallel ADC architecture where each sampled level is compared to a ramp level and the corresponding code is latched when a match is seen.

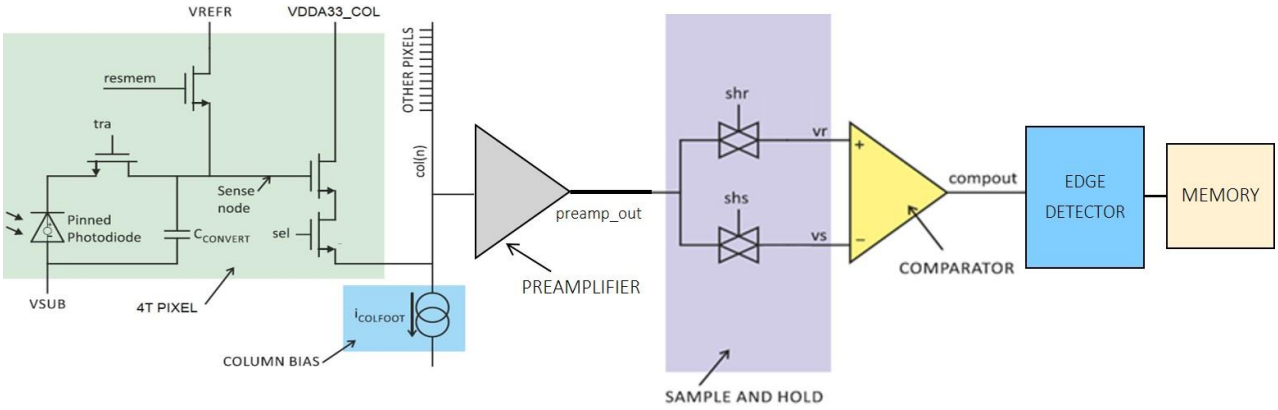

Figure 2. Readout path

The CIS124 uses a SPI (Serial Peripheral Interface) for configuring the image sensor, loading addresses for the readout of each row, configuring gain of each gain region, controlling test modes during characterisation.

In order to achieve the required frame rate the CIS124 must operate in pipeline operation, Figure 3, where the pixel access and AD conversion of each line runs concurrently with the read-out of the previous line, and with the SPI settings (gain & address) for the following line. The pixel access time is 7 µs and the readout path converts 8 rows in parallel in 2 µs . Each LVDS data output is clocked at 128 MHz in double data rate mode, giving 256 Mbps. The pixel readout process takes 12.6 µs for the 8 rows read in parallel which gives a frame rate of approximately 780 fps.

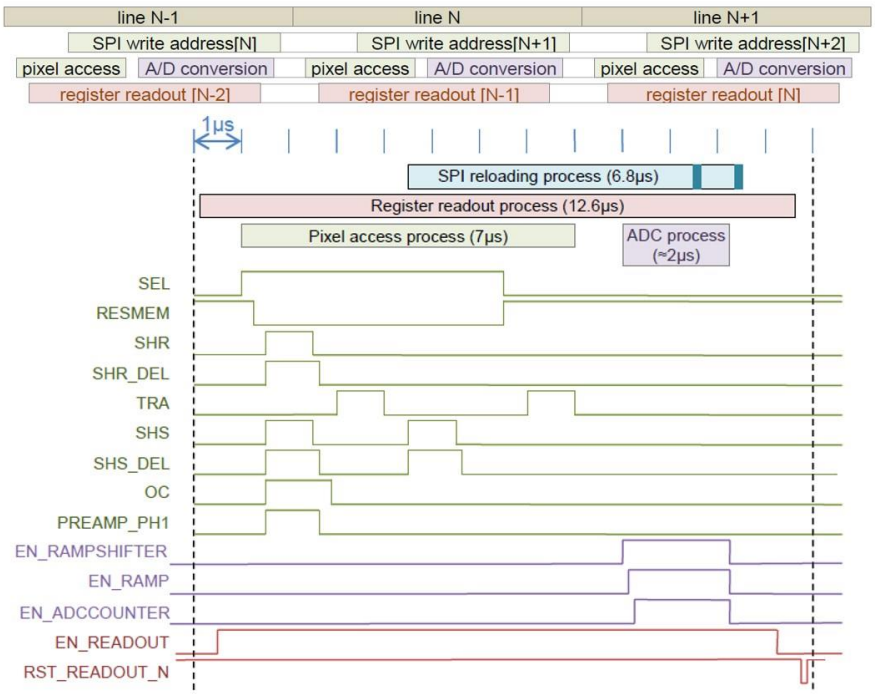

Figure 3. Timing access. Pipeline operation mode

3. PACKAGE DESIGN OVERVIEW

The LVSM package design, Figure 4, is suitable for both Front and Back side illuminated devices which allows evaluating the package design and developing the assembly procedures using front face chip samples while the back thinned devices are being manufactured. It consists of a Kovar base, two symmetrical tracked alumina ceramics (with 116 pins each), a window seal ring, electrical feedthroughs and a pump tube. The package contains a carrier mounted die which is cooled by a peltier cooler. Connections to the die are made via the tracked ceramics, with wire bonds used to make the electrical connections from the die to the ceramics. The temperature of the die is monitored by a temperature sensor which is wire bonded to one of the tracked ceramics. All of the internal mechanical joints are made with a thermally conductive adhesive in order to minimise the thermal resistance in the assembled LVSM. The package has a sapphire window with anti-reflected coating in order to meet the tight optical performance. This window is held inside a metallic frame to provide a surface for the customer to attach a lenslet array on top for WFS applications. The metallic frame in turn is seam sealed to the window frame of the package. The pump tube is used to evacuate and then back fill the internal volume with Krypton gas after the window has been attached to the package. An IPGA mounting bracket is glued to each of the tracked ceramics in order to provide threaded holes to be used to secure a connector from the customer system via a pair of jack screws. Figure 5 shows an exploded view of the assembly. Thermal and structural simulations have been carried out to guarantee that interface specifications were met.

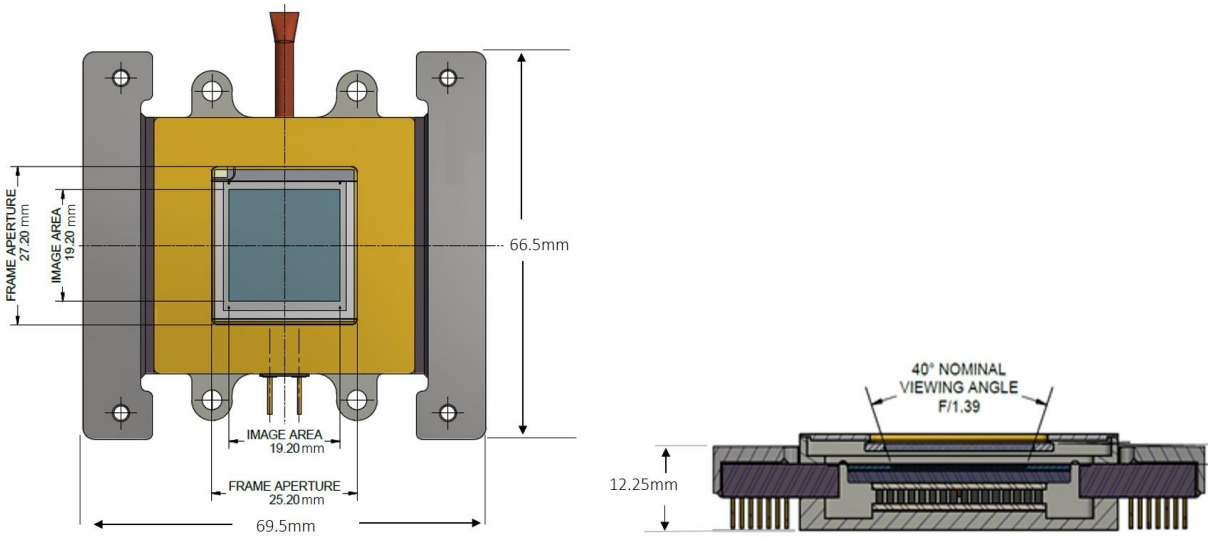

Figure 4. LVSM package design

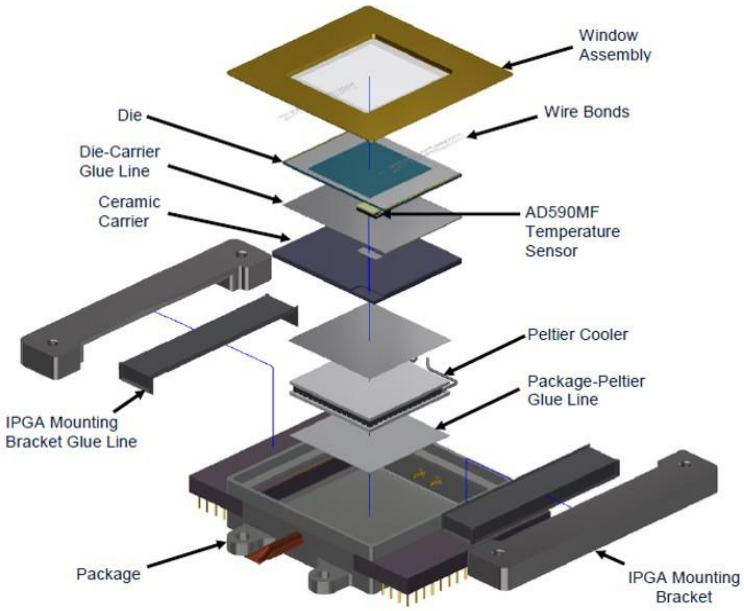

Figure 5. Exploded view of the LVSM package design

4. LVSM ASSEMBLY

4.1 Assembly

The assembly of the LVSMs has been carried out in Teledyne e2v's clean rooms and it follows a process very similar to other devices that Teledyne e2v have produced including the CCD220.

The brackets are attached to the package using an epoxy adhesive. This assembly is carried out in a jig to ensure that the jack screw holes on the IPGA Mounting Brackets are well aligned with the package, Figure 6. Then a Peltier cooler is glued in place to the package using conductive adhesive, Figure 7. This is then cured using a standard Teledyne e2v process. The position of the Peltier cooler is set by the plinth in the centre of the package, which allows consistent placement of the cooler. Once the adhesive is cured, the Peltier leads are resistance welded to the electrical feedthroughs.

The temperature sensor and the CMOS image die are then glued to the carrier which is then glued to the Peltier cooler, Figure 8. Once the carrier assembly is in place and the glue is fully cured the wire bonds are made to electrically connect the die and temperature sensor to the package. The wire bonding process is an ultrasonic wedge bonding process using 25µm aluminium-silicon bond wire.

The package is then windowed using the window assembly. The seal is made using a seam sealing process. The assembled LVSM is then connected to a pump station in order to evacuate it and it is back filled with Krypton. Krypton is the standard gas used in back filled packages due to its superior thermal properties. Once the package is back filled to

the required pressure, the pump tube is pinched off. This process deforms the pump tube and forms a cold weld across the tube. This hermetically seals the package.

The LVSM is inspected intensively throughout the assembly process. All parts are inspected prior to use in the assembly in order to ensure that no foreign material is present. After each assembly process is completed the assembly is given a brief inspection of relevant areas to ensure that it is being assembled correctly.

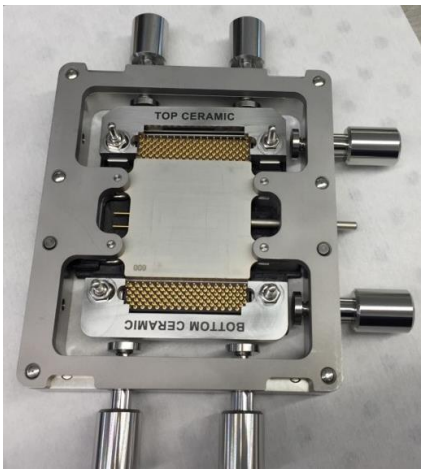

Figure 6. IPGA brackets attach to package using alignment jig

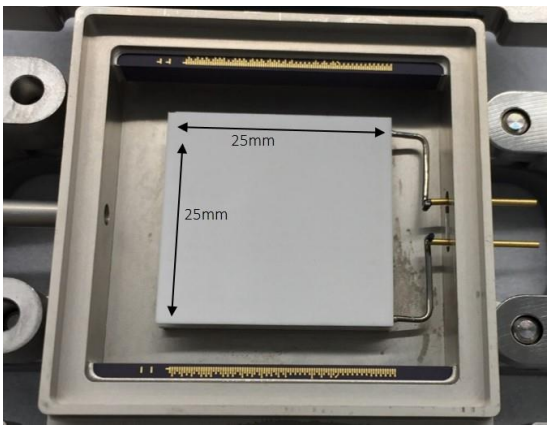

Figure 7. Peltier attach to package

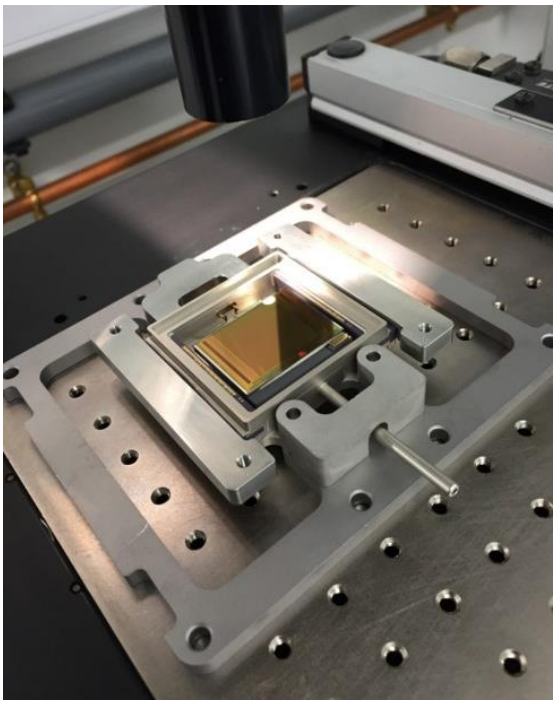

Figure 8. Carrier (with temperature sensor and CMOS die) attached to package.

Teledyne e2v has performed preliminary characterisation of the Peltier and confirmed the expected low power consumption (<0.5W) at nominal operating temperature of -5˚C point but can go down to -28˚ C when cooling the base of the package with water chill supply temp of 3°C. Table 2.

Table 2. LVSM Peltier performance

		Nominal Operating Condition	Minimum Temp Achievable
Chip Temperature		**-5˚C**	**-28˚C**
Device Peltier	Power	**0.495 W**	**9.28 W**
	Voltage	2 V	8.70 V
	Current	0.25 A	1.06
Chip Power Consumption		1.52 W	

Figure 9 shows the first two assembled devices using front face die with and without permanent window attached and Table 3 shows the initial geometrical results where we have successfully managed to meet the requirements in some cases by one order of magnitude.

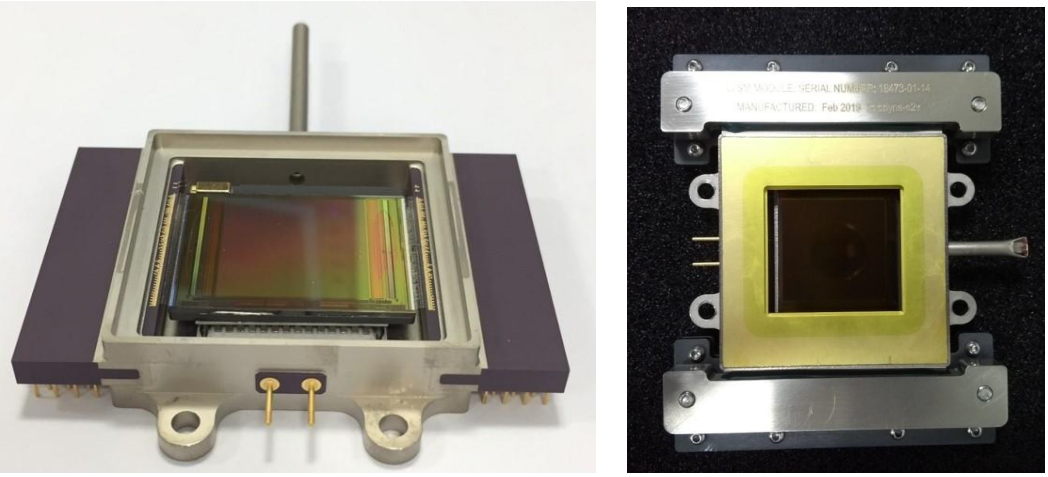

Figure 9. First LVSM – CIS124 devices assembled. Without permanent window (left) and with permanent window (right)

Table 3. Geometric Measurements

Parameter	Typical Value
Chip Flatness deviation	4 µm
Die to Window parallelism	0.074°
Window top surface to chip distance	2.9 mm

5. FRONT FACE PRELIMINARY CHARACTERISATION RESULTS

Specific test equipment has been developed to characterise the first front face devices which has been designed to be compatible also for testing back face devices. The test equipment has the following capabilities;

- Optics systems; Quartz halogen lamp, filter wheel, integrating sphere for uniform light distribution and LED for fast switching tests such as lag.
- Thermal control via Peltier and chill water supply.
- FPGA based stimulus and capture using COTS equipment.
- In-house Software for control of camera sub-systems.
- Two headboards used in the system, with identical PCB flipped on axis shown. Figure 10
- Programmable Voltage Supplies and Programmable Constant current.
- ZIF socketed sensor.
- Current monitoring circuits for sensor supplies.

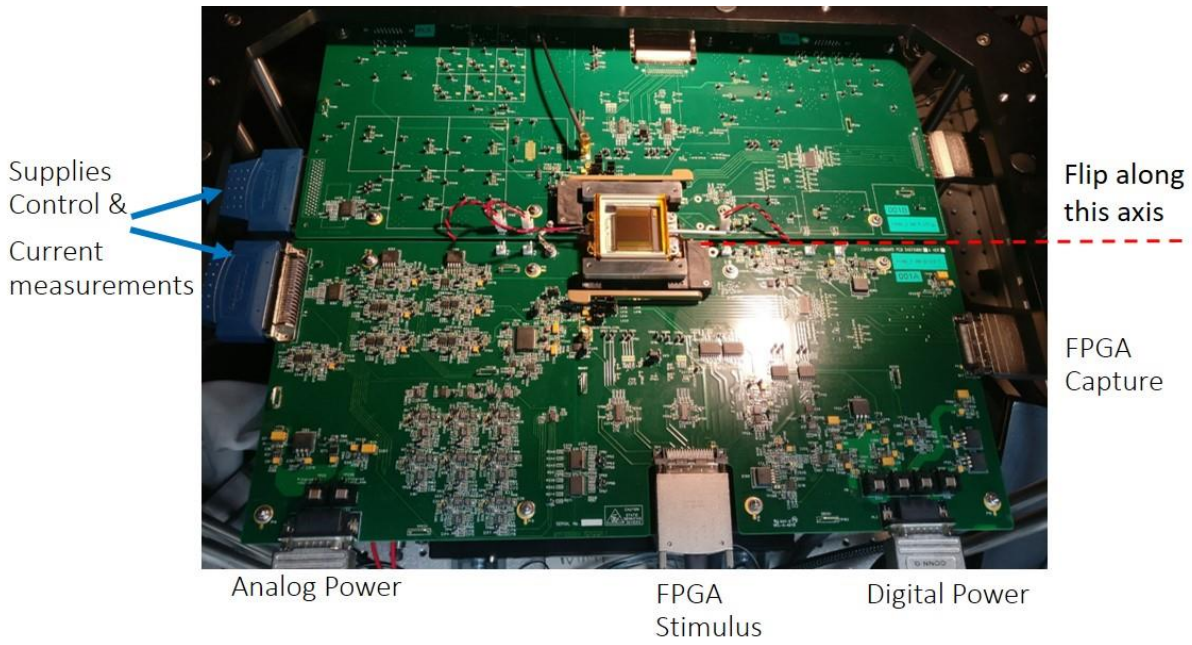

Figure 10. Headboard designed for driving both front and back face LVSM devices.

The test equipment described previously has allowed testing the front face devices assembled. Figure 11 shows the functional images captured at different gains. The chip power consumption has also been verified and is in line with expectations, 1.5 W. Images can be read out at full speed (128MHz) and column drive test mode shows good linearity behaviour for all four gain settings, <0.1%, see Figure 12.

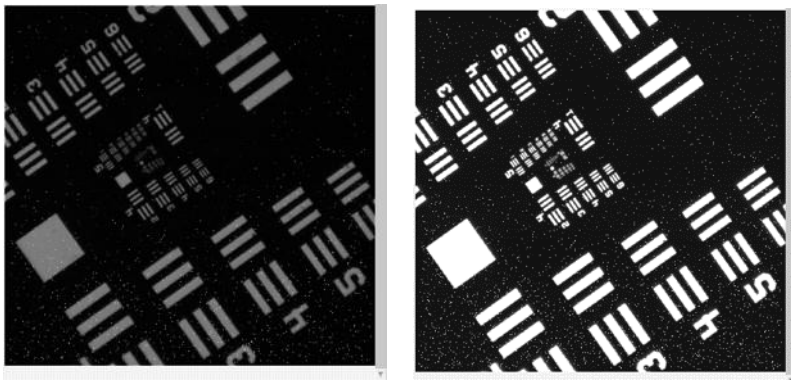

Figure 11. Functional images capture at gain 1 (left) and gain 8 (right)

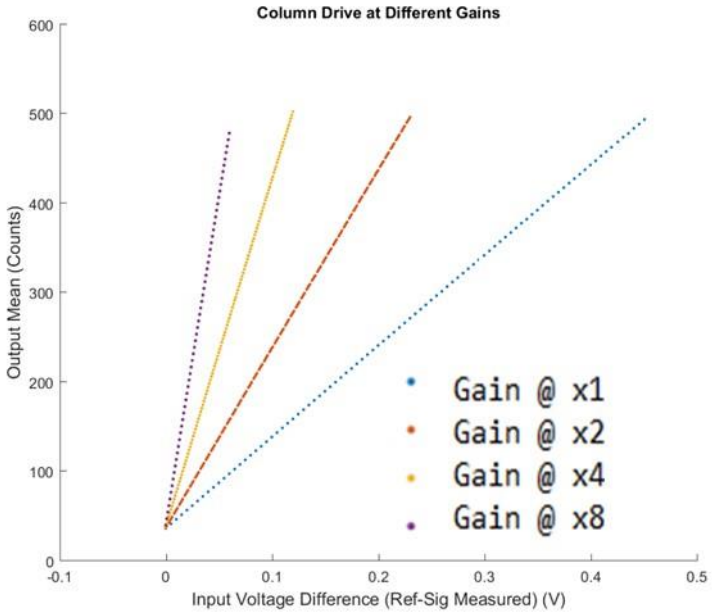

Figure 12. Column drive test mode showing good linearity behaviour for all four gain settings

Table 4 summaries the preliminary electro optical results obtained in pipeline operation on the front face device at ambient temperature, 20°C. These results have been obtained after initial optimization of the pixel and ADC timings and the multiple bias currents and are in line with the design predictions. We anticipate that gain 8 will be used for the smallest signals; although current readout noise (3.19e-) is slightly higher than predicted it is expected that after further optimization the noise value will be reduced to less than 3e- read noise.

Table 4. Preliminary EO results front face illuminated device at +20°C.

Gain	1	2	4	8
CCF Mean [ADU/e]	0.09	0.19	0.35	0.61
Relative Gain	1.0	2.0	3.9	6.7
Saturation [e-]	3339	1674	912	535
Linearity [%]	1.66	2.87	1.64	2.41
Readout Noise [e-]	6.35	3.97	3.38	3.19
Dark Signal [e-/s/pixel] at +20˚C	98.2	87.4	89.9	89.4

6. CONCLUSION

We have presented the design, assembly and initial characterisation results of the LVSM – CIS124 image sensor which are in line with prediction. The next step is to complete the characterisation of the backthinned devices that have being manufactured while the characterisation of the front face devices was carrying out. After development phase is completed with the characterisation of the backthinned device we will go into a production phase where a large number of sensors are planned to be delivered to ESO.